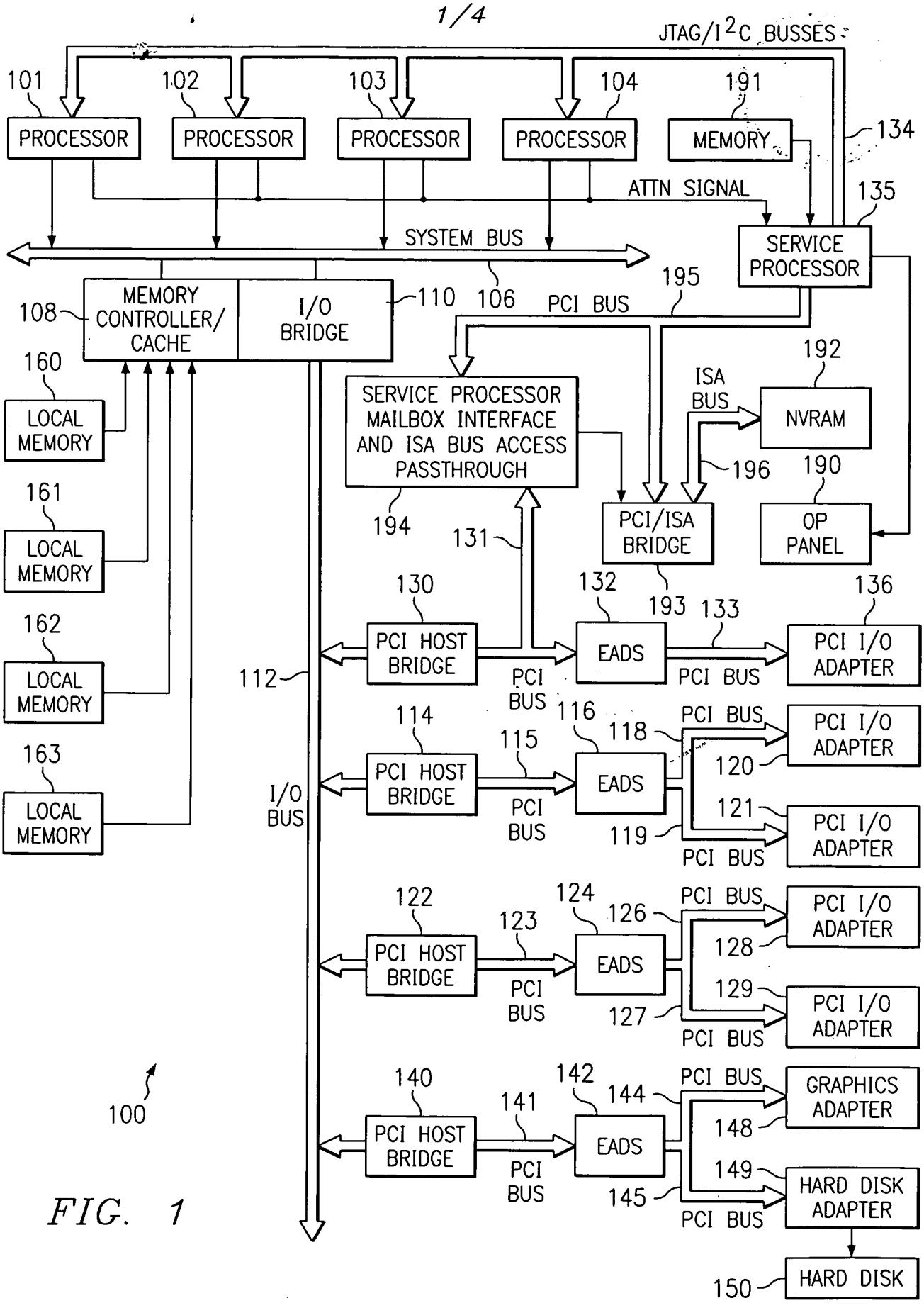

JTAG/I2C BUSSES
101
102
103
104
191
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
MEMORY
134
ATTN SIGNAL
135
SYSTEM BUS
SERVICE PROCESSOR
195
108
MEMORY CONTROLLER/ CACHE
I/O BRIDGE
110
106
PCI BUS
192
160
LOCAL MEMORY
SERVICE PROCESSOR MAILBOX INTERFACE AND ISA BUS ACCESS PASSTHROUGH
ISA BUS
NVRAM
196
190
161
LOCAL MEMORY
194
131
PCI/ISA BRIDGE
OP PANEL
130
132
193
133
136
162
LOCAL MEMORY
PCI HOST BRIDGE
EADS
PCI I/O ADAPTER
112
PCI BUS
PCI BUS
163
LOCAL MEMORY
114
116
118
PCI BUS
PCI I/O ADAPTER
115
120
PCI HOST BRIDGE
EADS
I/O BUS
PCI BUS
121
PCI I/O ADAPTER
119
PCI BUS
122
124
126
PCI BUS
PCI I/O ADAPTER
123
128
PCI HOST BRIDGE
EADS
PCI BUS
129
PCI I/O ADAPTER
127
PCI BUS
140
142
144
PCI BUS
GRAPHICS ADAPTER
141
148
PCI HOST BRIDGE
EADS
PCI BUS
149
HARD DISK ADAPTER
145
PCI BUS
HARD DISK
150
100

FIG. 1

FIG. 2

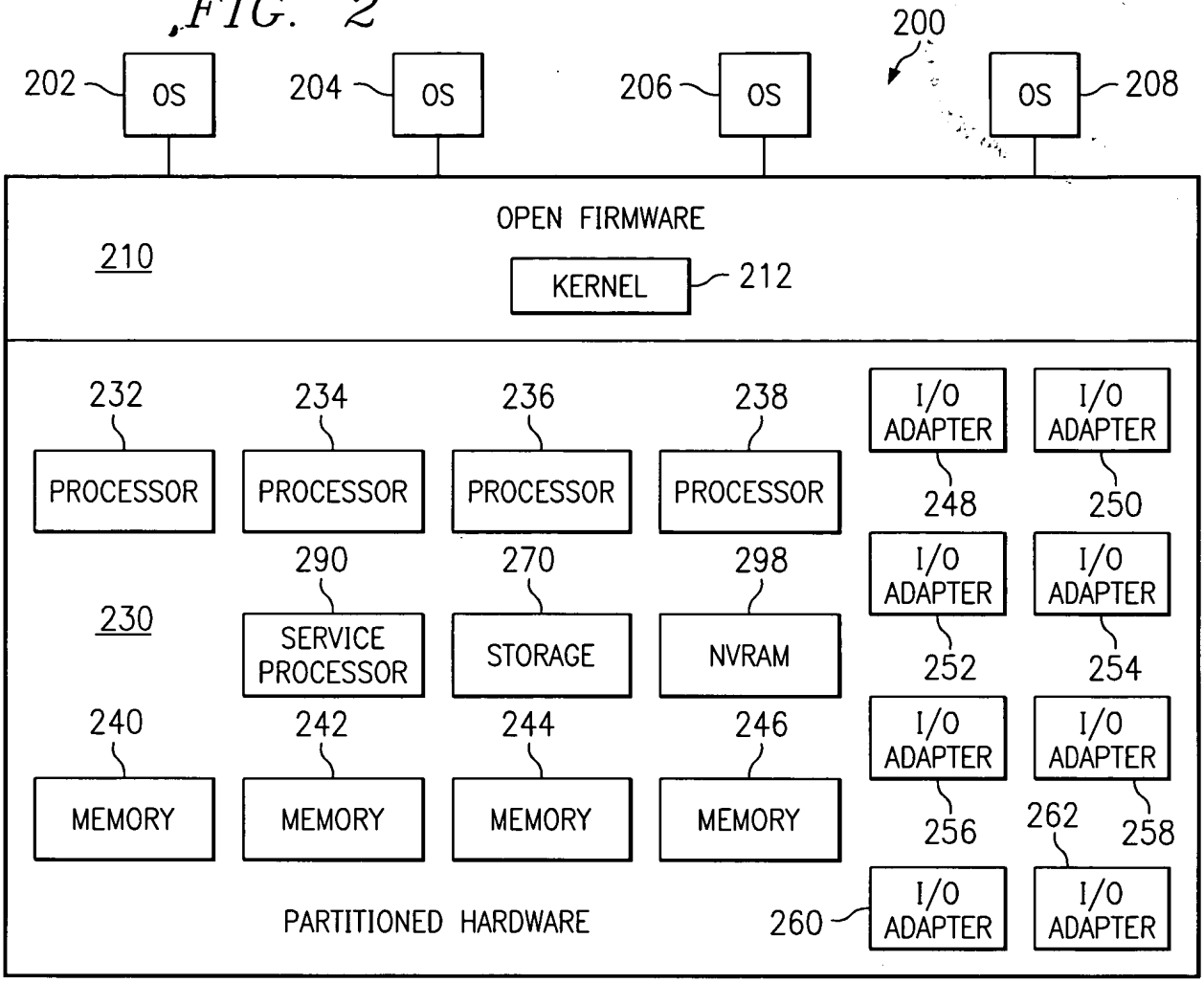
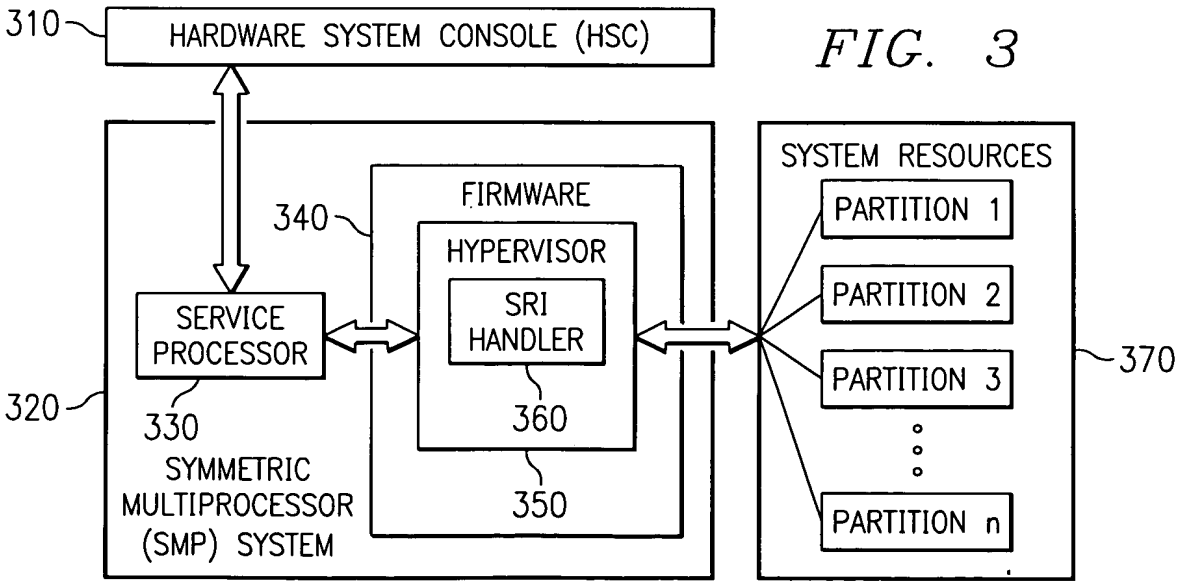

200
202
OS
204
OS
206
OS
OS
208
OPEN FIRMWARE
210
KERNEL
212
232
234
236
238
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
I/O ADAPTER
I/O ADAPTER
248
250
290
270
298
230
SERVICE PROCESSOR
STORAGE
NVRAM
I/O ADAPTER
I/O ADAPTER
252
254
240
242
244
246
MEMORY
MEMORY
MEMORY
MEMORY
I/O ADAPTER
I/O ADAPTER
256
262
258
I/O ADAPTER
I/O ADAPTER
260
PARTITIONED HARDWARE

FIG. 3


310
HARDWARE SYSTEM CONSOLE (HSC)
SYSTEM RESOURCES
FIRMWARE
340
HYPERVISOR
SRI HANDLER
PARTITION 1
PARTITION 2
PARTITION 3
PARTITION n
370
SERVICE PROCESSOR
320
330
360
350
SYMMETRIC MULTIPROCESSOR (SMP) SYSTEM

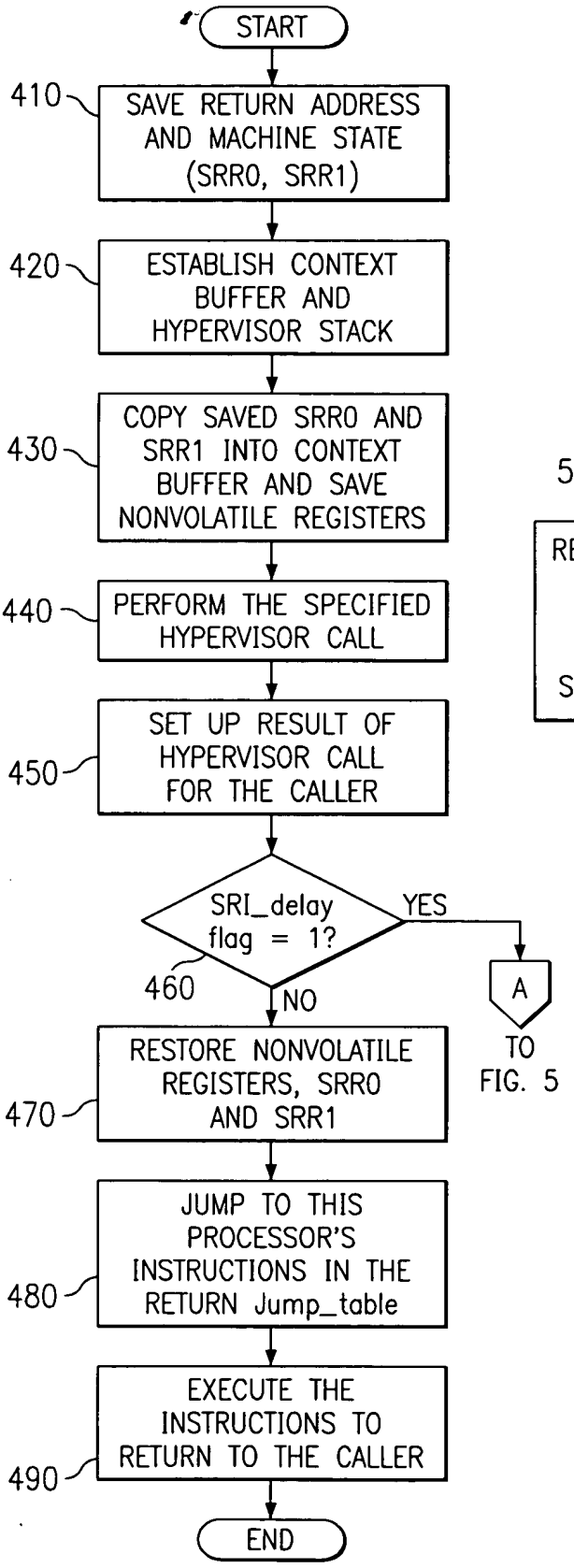

START
410
SAVE RETURN ADDRESS AND MACHINE STATE (SRR0, SRR1)
420
ESTABLISH CONTEXT BUFFER AND HYPERVISOR STACK
430
COPY SAVED SRR0 AND SRR1 INTO CONTEXT BUFFER AND SAVE NONVOLATILE REGISTERS
440
PERFORM THE SPECIFIED HYPERVISOR CALL
450
SET UP RESULT OF HYPERVISOR CALL FOR THE CALLER
SRI_delay flag = 1?
460
YES
NO
A
TO FIG. 5
470
RESTORE NONVOLATILE REGISTERS, SRR0 AND SRR1
480
JUMP TO THIS PROCESSOR'S INSTRUCTIONS IN THE RETURN Jump_table
490
EXECUTE THE INSTRUCTIONS TO RETURN TO THE CALLER
END

FIG. 4

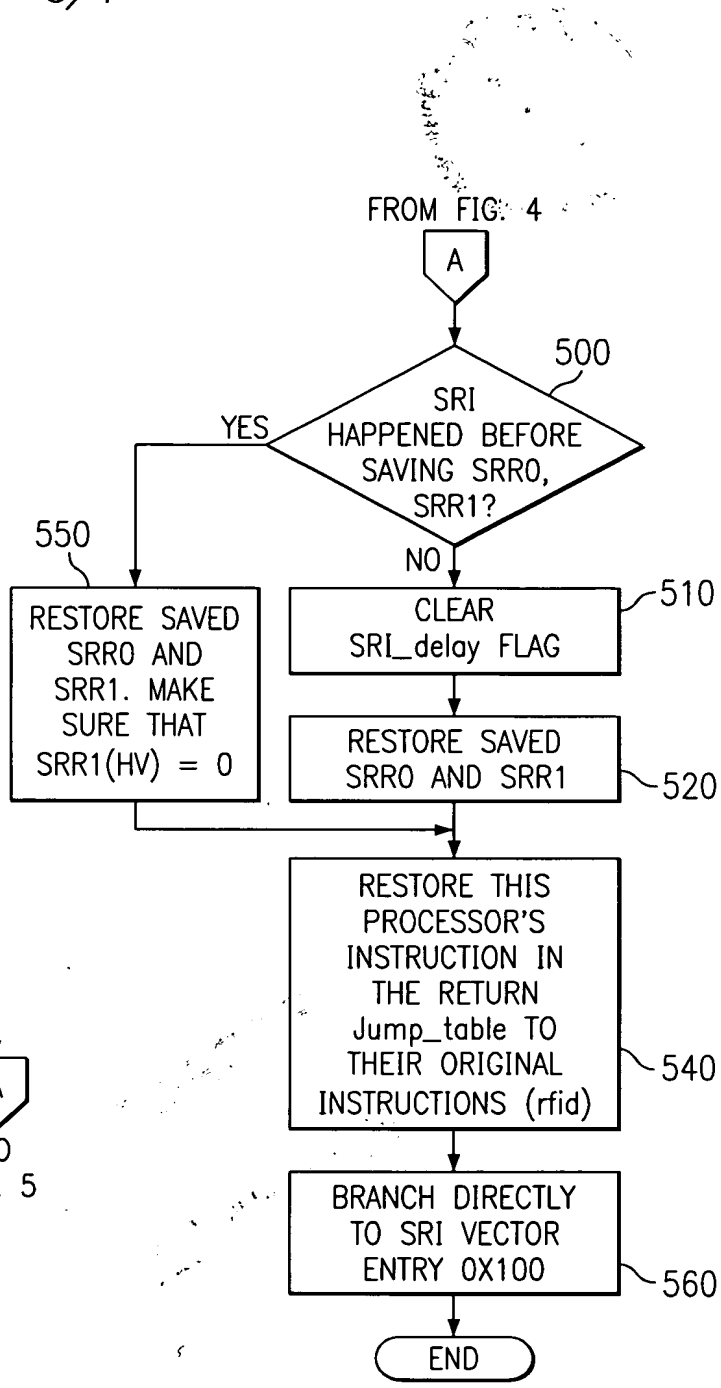
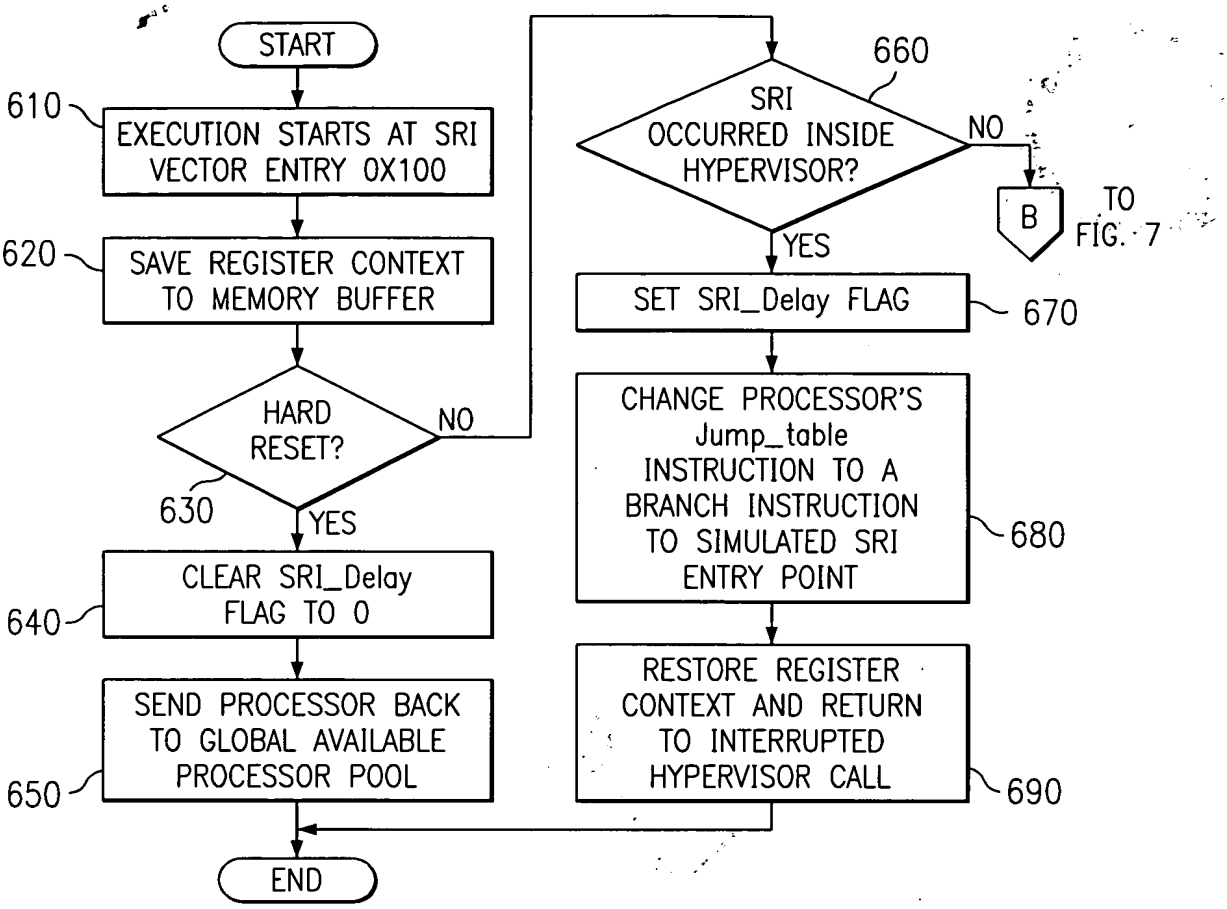

FROM FIG. 4
A
500
SRI HAPPENED BEFORE SAVING SRR0, SRR1?
YES
NO
550
RESTORE SAVED SRR0 AND SRR1. MAKE SURE THAT SRR1(HV) = 0
510
CLEAR SRI_delay FLAG
RESTORE SAVED SRR0 AND SRR1
520
RESTORE THIS PROCESSOR'S INSTRUCTION IN THE RETURN Jump_table TO THEIR ORIGINAL INSTRUCTIONS (rfid)
540
BRANCH DIRECTLY TO SRI VECTOR ENTRY 0X100
560
END

FIG. 5

FIG. 6


START
610
EXECUTION STARTS AT SRI VECTOR ENTRY 0X100
620
SAVE REGISTER CONTEXT TO MEMORY BUFFER
HARD RESET?
NO
630
YES
640
CLEAR SRI_Delay FLAG TO 0
650
SEND PROCESSOR BACK TO GLOBAL AVAILABLE PROCESSOR POOL
END
660
SRI OCCURRED INSIDE HYPERVISOR?
NO
B
TO FIG. 7
YES
SET SRI_Delay FLAG
670
CHANGE PROCESSOR'S Jump_table INSTRUCTION TO A BRANCH INSTRUCTION TO SIMULATED SRI ENTRY POINT
680
RESTORE REGISTER CONTEXT AND RETURN TO INTERRUPTED HYPERVISOR CALL
690

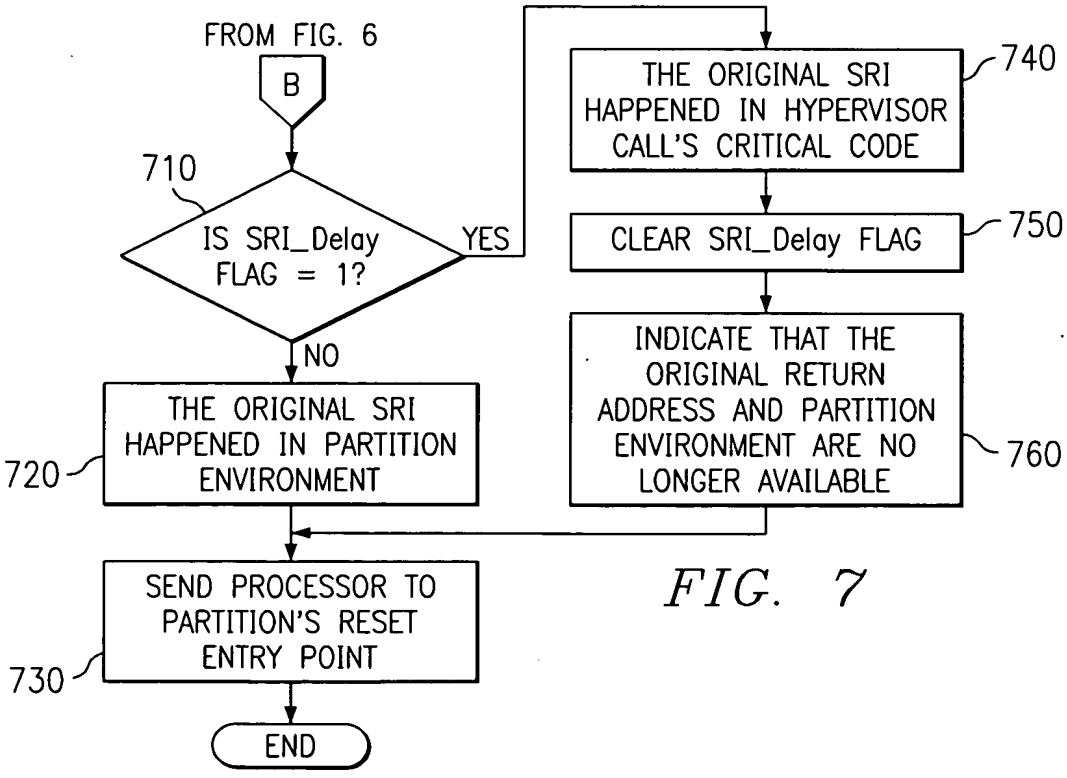

FROM FIG. 6
B
710
IS SRI_Delay FLAG = 1?
YES
NO
720
THE ORIGINAL SRI HAPPENED IN PARTITION ENVIRONMENT
730
SEND PROCESSOR TO PARTITION'S RESET ENTRY POINT
END
740
THE ORIGINAL SRI HAPPENED IN HYPERVISOR CALL'S CRITICAL CODE
750
CLEAR SRI_Delay FLAG
760
INDICATE THAT THE ORIGINAL RETURN ADDRESS AND PARTITION ENVIRONMENT ARE NO LONGER AVAILABLE

FIG. 7